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(54) **DEMUX DISPLAY PANEL AND OLED DISPLAY**

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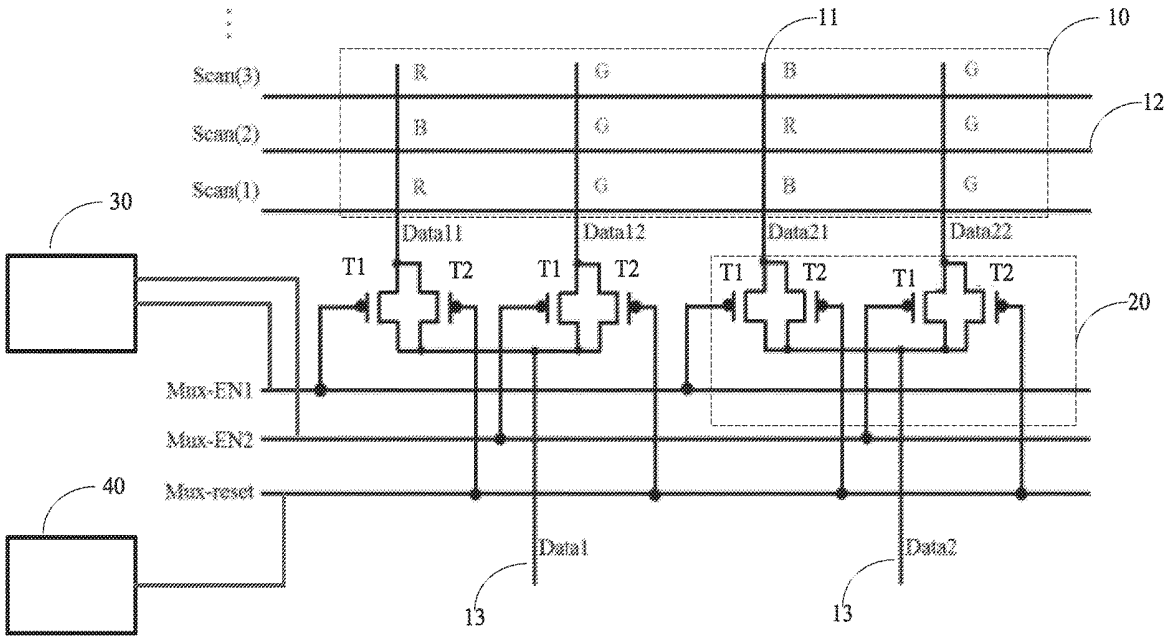
(57) **ABSTRACT**

A demultiplexer (DEMUX) display panel comprising an array substrate, a plurality of DEMUX switches, and a second control signal generating circuit which is connected to a second control signal input terminal and is configured to generate a second control signal. The second control signal is sent to the DEMUX switch before scanning each row of the sub-pixels to make the DEMUX switch transmit a reset signal to the corresponding first data lines through both of the data signal output terminals.



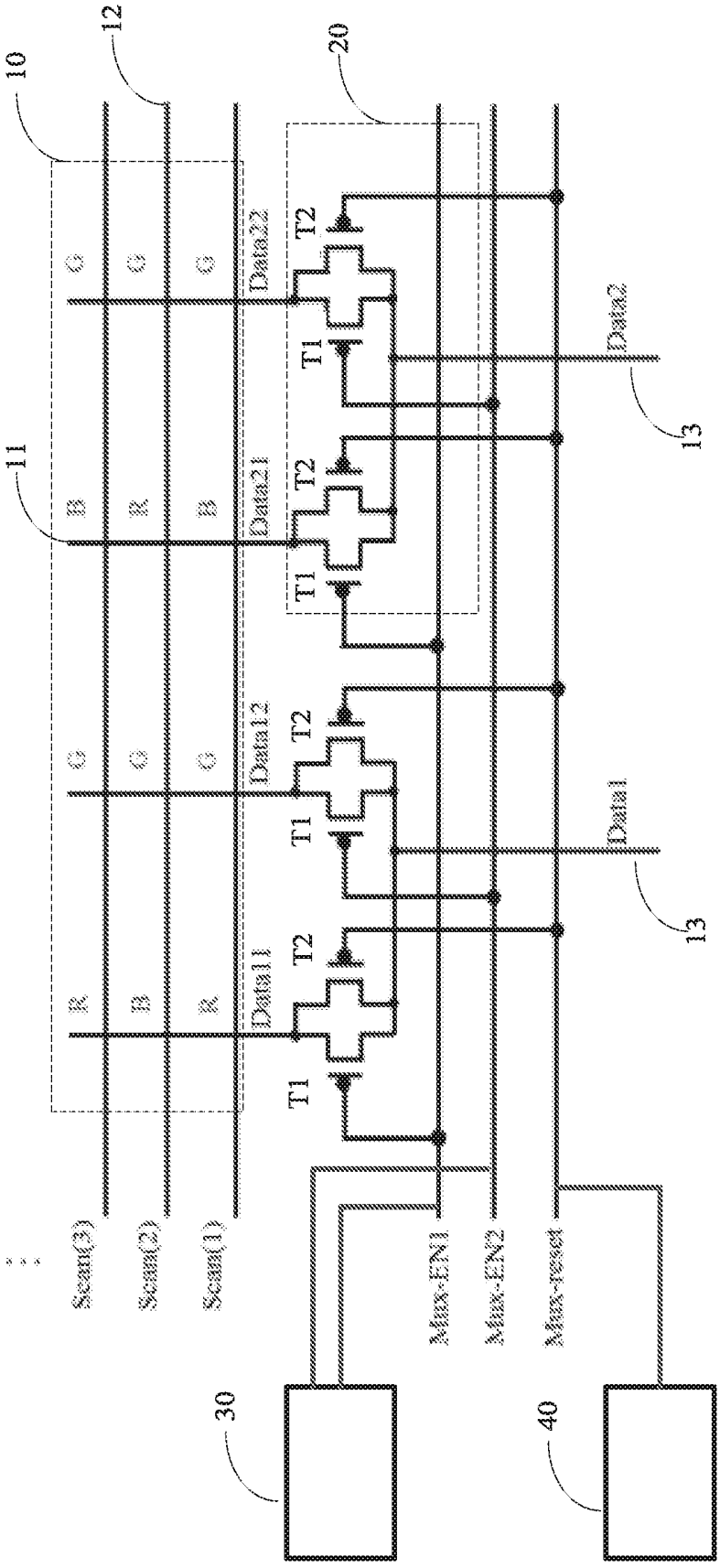

10
12
20
11
13
13
30
40
G
G
G
B
R
B
R
B
R
Data22
Data21
Data12
Data11
T1
T2
Data2
Data1
Scan(3)
Scan(2)
Scan(1)
Mux-EN1
Mux-EN2
Mux-reset

FIG. 1

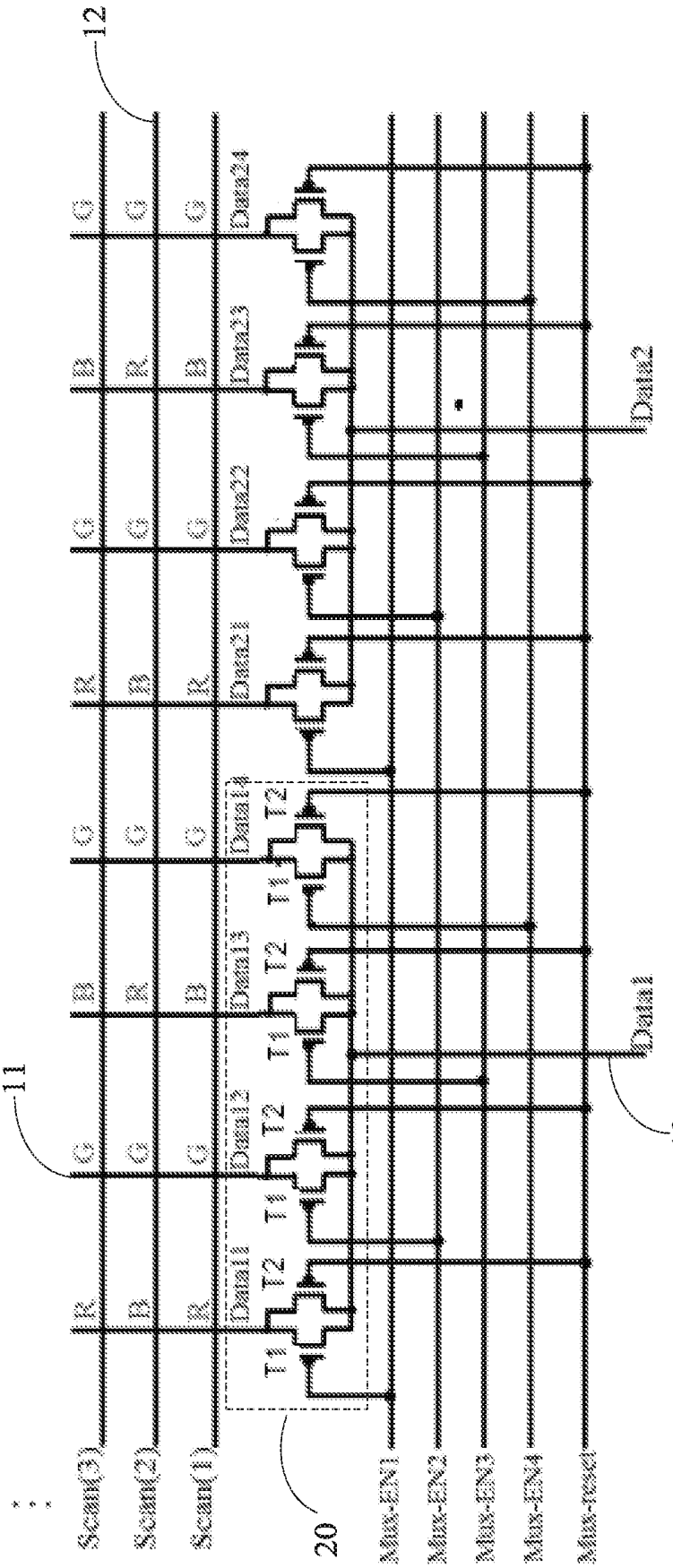

12
11
13
20
Data1
Data2
Data11
Data12
Data13
Data14
Data21
Data22
Data23
Data24
Scan(3)
Scan(2)
Scan(1)
Mux-EN1
Mux-EN2
Mux-EN3
Mux-EN4
Mux-reset
T1
T2
R
G
B

FIG. 2

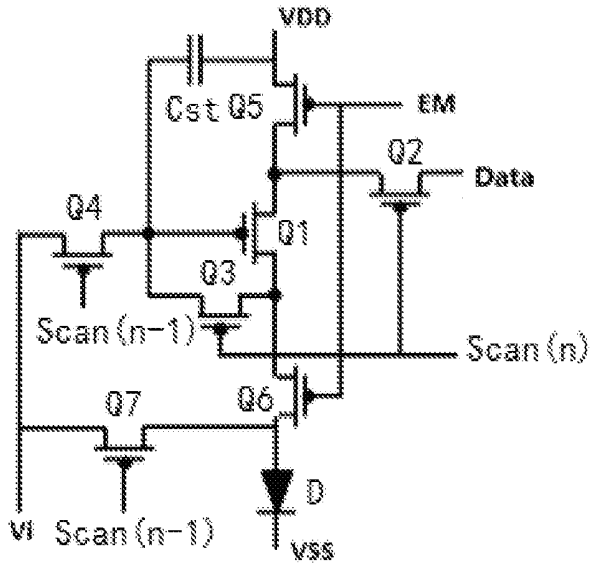

VDD
Cst
Q5
EM
Q2
Data
Q4
Q1
Q3
Scan(n-1)
Scan(n)
Q7
Q6
D
VI
Scan(n-1)
Vss

FIG. 3

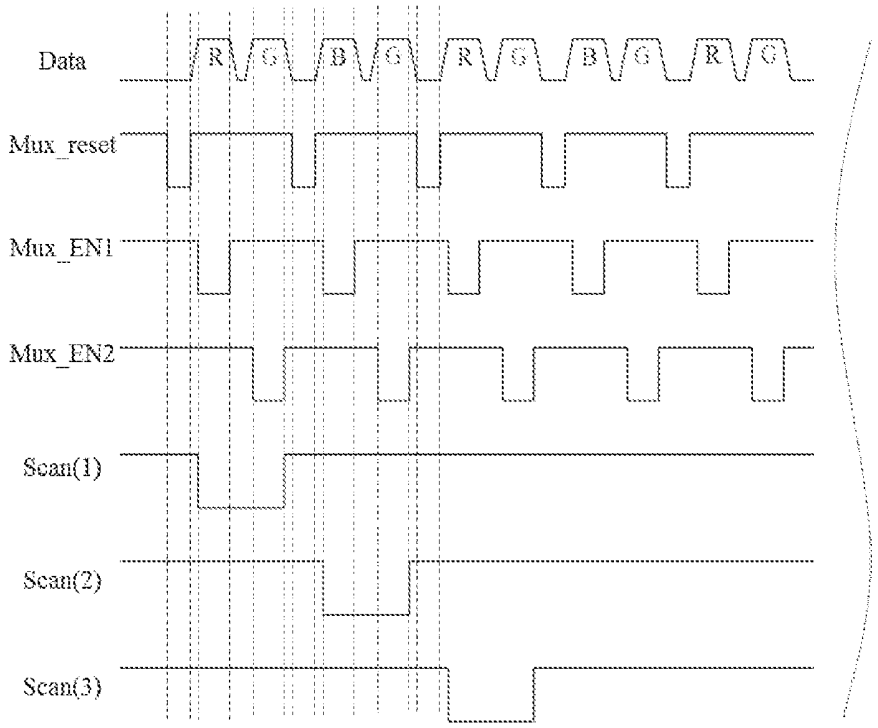

Data
R
G
B
G
R
G
B
G
R
G
Mux_reset
Mux_EN1
Mux_EN2
Scan(1)
Scan(2)
Scan(3)

FIG. 4

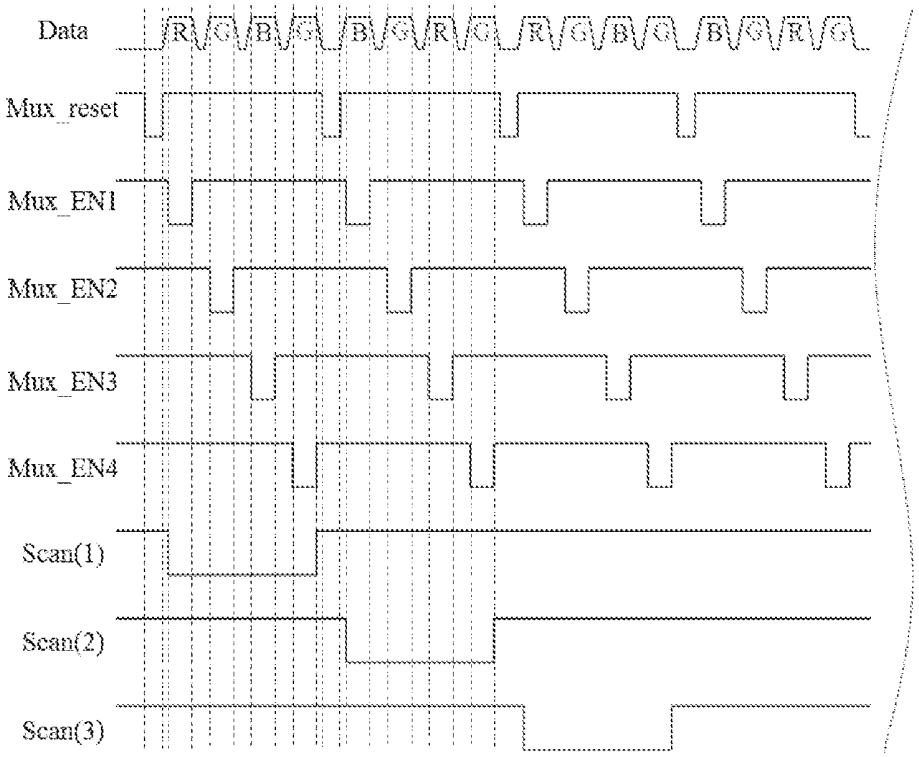

Data
R
G
B
G
B
G
R
G
R
G
B
G
B
G
R
G
Mux_reset
Mux_EN1
Mux_EN2
Mux_EN3
Mux_EN4
Scan(1)
Scan(2)
Scan(3)

FIG. 5

DEMUX DISPLAY PANEL AND OLED DISPLAY

FIELD OF INVENTION

[0001] The present disclosure relates to liquid crystal displays (LCDs), and in particular to a demultiplexer (DEMUX) LCD panel and an organic light-emitting diode (OLED) display.

BACKGROUND OF INVENTION

[0002] OLEDs have broad gamut, high contrast, low power consumption and flexibility, thus OLEDs have high competitiveness in display area. Active-matrix organic light-emitting diodes (AMOLEDs) are a target field in developing flexible displays. A driving circuit of AMOLED is 2T1C structure which includes a switch thin film transistor, a driving thin film transistor, and a storage capacitor.

[0003] However, in present OLED display panels, current DEMUX circuits and time sequences have disadvantages, such as data signals cannot be written as usually and will result in display error.

[0004] Therefore, the disadvantages exist in present technologies require urgent improvements.

SUMMARY OF INVENTION

[0005] The objection of the present disclosure is proving a DENUS display panel and an OLED display to improve the display error.

[0006] A demultiplexer (DEMUX) display panel, comprising:

[0007] an array substrate comprising a pixel area defined by a plurality of first data lines intersecting a plurality of scan lines, wherein the pixel area comprises sub-pixels;

[0008] a plurality of DEMUX switches, each of the DEMUX switches comprising at least one data signal input terminal, at least two data signal output terminals, at least two first control signal input terminals, and a second control signal input terminal, wherein a corresponding second data line connects to the data signal input terminal, the corresponding first data line connects between the at least two data signal output terminals and at least two of the sub-pixels;

[0009] a first control signal generating circuit connected to the at least two first control signal input terminals, and configured to generate a first control signal, wherein the first control signal is sent to one of the corresponding first control signal input terminals to make the DEMUX switch transmit a data signal to the corresponding sub-pixels through a corresponding data signal output terminal;

[0010] a second control signal generating circuit connected to the second control signal input terminal, and configured to generate a second control signal, wherein the second control signal is sent to the DEMUX switch before scanning the sub-pixels to make the DEMUX switch transmit a reset signal to the corresponding first data line through both of the data signal output terminals;

[0011] wherein the DEMUX switch comprises at least two first transistors and at least two second transistors;

[0012] wherein an input terminal of the first transistor connects to the corresponding second data line, an output terminal of the first transistor connects to one of the corresponding data line and the corresponding sub-pixels, a gate of the first transistor connects to the first control signal generating circuit;

[0013] wherein the input terminals of both of the first transistor connect to input terminals of one of the second transistors, the output terminals of both of the first transistor connects to output terminals of the corresponding second transistors, gates of the at least two second transistors connect to each other to receive the second control signal;

[0014] each of the DEMUX switches comprises two data signal output terminals connected to two different colored sub-pixels.

[0015] In the DEMUX display panel of the present disclosure, the first transistor and the second transistor are N-type field-effect transistors.

[0016] In the DEMUX display panel of the present disclosure, the two different colored sub-pixels are a red sub-pixel and a green sub-pixel, or the two different colored sub-pixels are a blue sub-pixel and a green sub-pixel.

[0017] In the DEMUX display panel of the present disclosure, the data signal output terminals of the DEMUX switches transmit low potential voltages as the reset signals to the corresponding second data lines before scan lines receive scan signals.

[0018] In the DEMUX display panel of the present disclosure, each of the DEMUX switches comprises four data signal output terminals connected to a red sub-pixel, a blue sub-pixel and two green sub-pixels.

[0019] In the DEMUX display panel of the present disclosure, each of the DEMUX switches comprises three data signal output terminals connected to a red sub-pixel, a blue sub-pixel and a green sub-pixel.

[0020] In the DEMUX display panel of the present disclosure, each of the sub-pixels comprises a first thin film transistor, a second thin film transistor, a third thin film transistor, a fourth thin film transistor, a fifth thin film transistor, a sixth thin film transistor, a seventh thin film transistor, an organic light-emitting diode, and a storage capacitor;

[0021] wherein an input terminal of the fourth thin film transistor and an input terminal of the seventh thin film transistor receive a Vi voltage, an output terminal of the fourth thin film transistor connects to a first terminal of the storage capacitor, a gate of the first thin film transistor and an input terminal of the third thin film transistor, a gate of the fourth thin film transistor and a gate of the seventh thin film transistor connect to an (n−1)th scan line, the output terminal of the fourth thin film transistor and an output terminal of the seventh thin film transistor connect to the organic light-emitting diode and an output terminal of the sixth thin film transistor, a second terminal of the storage capacitor connects to an input terminal of the fifth thin film transistor and receives a VDD voltage, an output terminal of the fifth thin film transistor and an output terminal of the second thin film transistor connect to an input terminal of the first thin film transistor, in output terminal of the first thin film transistor connects to an output terminal of the third thin film transistor and an input terminal of the sixth thin film transistor, a gate of the fifth thin film transistor connects to a gate of the sixth thin film transistor, a gate terminal of the second

thin film transistor connects to a gate of the third thin film transistor and the (n)th scan line, an input terminal of the second thin film transistor connects to one of the corresponding first data lines.

[0022] A demultiplexer (DEMUX) display panel, comprising:

[0023] an array substrate comprising a pixel area defined by a plurality of first data lines intersecting a plurality of scan lines, wherein the pixel area comprises sub-pixels;

[0024] a plurality of DEMUX switches, each of the DEMUX switches comprising at least one data signal input terminal, at least two data signal output terminals, at least two first control signal input terminals, and a second control signal input terminal, wherein a corresponding second data line connects to the data signal input terminal, the corresponding first data line connects between the at least two data signal output terminals and at least two of the sub-pixels;

[0025] a first control signal generating circuit connected to the at least two first control signal input terminals, and con figured to generate a first control signal, wherein the first control signal is sent to one of the corresponding first control signal input terminals to make the DEMUX switch transmit a data signal to the corresponding sub-pixels through a corresponding data signal output terminal;

[0026] a second control signal generating circuit connected to the second control signal input terminal, and con figured to generate a second control signal, wherein the second control signal is sent to the DEMUX switch before scanning the sub-pixels to make the DEMUX switch transmit a reset signal to the corresponding first data lines through both of the data signal output terminal.

[0027] In the DEMUX display panel of the present disclosure, the DEMUX switch comprises at least two first transistors and at least two second transistors; wherein an input terminal of the first transistor connects to the corresponding second data line, an output terminal of the first transistor connects to one of the corresponding data line and the corresponding sub-pixels, a gate of the first transistor connects to the first control signal generating circuit;

[0028] wherein the input terminals of both of the first transistor connect to input terminals of the second transistors, the output terminals of both of the first transistor connect to output terminals of the corresponding second transistors, gates of the at least two second transistors connect to each other to receive the second control signal.

[0029] In the DEMUX display panel of the present disclosure, the first transistors and the second transistors are N-type field-effect transistors.

[0030] In the DEMUX display panel of the present disclosure, each of the DEMUC switches comprises two data signal output terminals connected to two different colored sub-pixels.

[0031] In the DEMUX display panel of the present disclosure, the two different colored sub-pixels are a red sub-pixel and a green sub-pixel, or the two different colored sub-pixels are a blue sub-pixel and a green sub-pixel.

[0032] In the DEMUX display panel of the present disclosure, the data signal output terminals of the DEMUX switches transmit low potential voltages as the reset signals to the corresponding second data lines before scan lines receive scan signals.

[0033] In the DEMUX display panel of the present disclosure, each of the DEMUX switches comprises four data signal output terminals connected to a red sub-pixel, a blue sub-pixel and two green sub-pixels.

[0034] In the DEMUX display panel of the present disclosure, each of the DEMUX switches comprises three data signal output terminals connected to a red sub-pixel, a blue sub-pixel and a green sub-pixel.

[0035] In the DEMUX display panel of the present disclosure, each of the sub-pixels comprises a first thin film transistor, a second thin film transistor, a third thin film transistor, a fourth thin film transistor, a fifth thin film transistor, a sixth thin film transistor, a seventh thin film transistor, an organic light-emitting diode, and a storage capacitor; wherein an input terminal of the fourth thin film transistor and an input terminal of the seventh thin film transistor receive a Vi voltage, an output terminal of the fourth thin film transistor connects to a first terminal of the storage capacitor, a gate of the first thin film transistor and an input terminal of the third thin film transistor, a gate of the fourth thin film transistor and a gate of the seventh thin film transistor connect to an (n−1)th scan line, the output terminal of the fourth thin film transistor and an output terminal of the seventh thin film transistor connect to the organic light-emitting diode and an output terminal of the sixth thin film transistor, a second terminal of the storage capacitor connects to an input terminal of the fifth thin film transistor and receives a VDD voltage, an output terminal of the fifth thin film transistor and an output terminal of the second thin film transistor connect to an input terminal of the first thin film transistor, in output terminal of the first thin film transistor connects to an output terminal of the third thin film transistor and an input terminal of the sixth thin film transistor, a gate of the fifth thin film transistor connects to a gate of the sixth thin film transistor, a gate of the second thin film transistor connects to a gate of the third thin film transistor and the (n)th scan line, an input terminal of the second thin film transistor connects to one of the first data lines.

[0036] A organic light-emitting diode (OLED) display comprising a demultiplexer (DEMUX) display panel,

[0037] the DEMUX display panel comprises:

[0038] an array substrate comprising a pixel area defined by a plurality of first data lines intersecting a plurality of scan lines, wherein the pixel area comprises sub-pixels;

[0039] a plurality of DEMUX switches, each of the DEMUX switches comprising at least one data signal input terminal, at least two data signal output terminals, at least two first control signal input terminals, and a second control signal input terminal, wherein a corresponding second data line connects to the data signal input terminal, the corresponding first data line connects between the at least two data signal output terminals and at least two of the sub-pixels;

[0040] a first control signal generating circuit connected to the at least two first control signal input terminals, and con figured to generate a first control signal, wherein the first control signal is sent to one of the corresponding first control signal input terminals to

make the DEMUX switch transmit a data signal to the corresponding sub-pixels through a corresponding data signal output terminal;

[0041] a second control signal generating circuit connected to the second control signal input terminal, and con figured to generate a second control signal, wherein the second control signal is sent to the DEMUX switch before scanning the sub-pixels to make the DEMUX switch transmit a reset signal to the corresponding first data lines through both of the data signal output terminal.

[0042] In the DEMUX display panel of the present disclosure, the DEMUX switch comprises at least two first transistors and at least two second transistors;

[0043] wherein an input terminal of the first transistor connects to the corresponding second data line, an output terminal of the first transistor connects to one of the corresponding data line and the corresponding sub-pixels, a gate of the first transistor connects to the first control signal generating circuit;

[0044] wherein the input terminals of both of the first transistor connect to input terminals of one of the second transistors, the output terminals of both of the first transistor connect to output terminals of the corresponding second transistors, gates of the at least two second transistors connect to each other to receive the second control signal.

[0045] In the DEMUX display panel of the present disclosure, the first transistors and the second transistors are N-type field-effect transistor.

[0046] In the DEMUX display panel of the present disclosure, each of the DEMUX switches comprises two data signal output terminals connected to two different colored sub-pixels.

[0047] The present disclosure utilizing the second control signal generating circuit, which is connected to the second control signal input terminal, to generate and transmit the second control signal to the DEMUX switch before starting scanning each rows of the sub-pixels, so that the DEMUX switch sent the reset signals to the corresponding first data lines in the purpose of resetting the corresponding first data lines. Thus, the error happening during writing the data signals into the first data lines that resulted from the higher voltage potential of the (n−1)th first data line in comparison with the voltage potential of the nth first data line. As the result, the problems of displaying errors are solved.

[0048] To clarify the technology method of the embodiments of the present disclosure, the following context will introduce the drawings representing the embodiments of the present disclosure. Obviously, the described drawings are only a part but not all of the drawings for exemplifying the present invention instead of limiting the present invention. For a skilled person in the art, other drawings may be obtained by referencing the drawings of the present disclosure without creative efforts.

DESCRIPTION OF THE DRAWINGS

[0049] FIG. **1** illustrates a structure of a first embodiment of a DEMUX display panel of the present disclosure.

[0050] FIG. **2** illustrates a structure of a second embodiment of a DEMUX display panel of the present disclosure.

[0051] FIG. **3** illustrates a structure of a sub-pixel of the DEMUX display panel of the present disclosure.

[0052] FIG. **4** illustrates a time sequence of the first embodiment of the DEMUX display panel as shown in FIG. **1**.

[0053] FIG. **5** illustrates a time sequence of the second embodiment of the DEMUX display panel as shown in FIG. **2**.

DETAILED DESCRIPTION OF PREFERRED EMBODIMENTS

[0054] To further illustrate the technical methods adopted by the present invention and the effects thereof, the following describes the preferable embodiments of the present invention and the accompanying drawings in detail. In the drawings, units having the same or similar structures are numbered the same or similar. The described embodiments accompanying with drawings are examples rather than limitations for explaining the present.

[0055] The illustrations of the following embodiments take the attached drawings as reference to indicate the applicable specific examples of the present disclosure. The mentioned directional terms, such as central, vertical, horizontal, length, width, upper, lower, front, back, left, right, inner, perpendicular, plane, top, bottom, outer, clockwise, anti-clockwise, etc., are only directions by referring to the accompanying drawings, and thus the used directional terms are used to describe and understand the present invention, but the present invention is not limited thereto. In addition, the terms "first" or "second" are only descriptive, not for indicating the relevant importance or the numbers of technical features. Therefore, the features containing "first" and "second" could be indicative inclusion of one or more such features. In the description of present disclosure, "plurality" means two or more, unless there are additional instructions.

[0056] In the specification of present disclosure, the terms install, connect, link should be explain as broad as possible unless there are specific rules or limitations. For example, connection can be fixed connection, removable connection or integral connection; link can be electrical coupling or communication; connection can be direct connection, indirect connection via a media, and connection between two inner components or mutual affection between two components. For a skilled person in the art, the above-mentioned term can be understood according to the practical conditions in the present disclosure.

[0057] In the present disclosure, unless there are specific rules or limitations, the description "the first feature is above or under the second feature" includes situations that the first feature directly contact the second feature or the first feature indirectly contact the second feature via a media. In addition, the description "the first feature is above the second feature" includes situations that the first feature is right above the second feature, the first feature in the incline top of the second feature, or the vertical height of the first feature is higher than the vertical height of the second feature. The description "the first feature is under the second feature" includes situations that the first feature is right below the second feature, the first feature in the oblique bellow of the second feature, or the vertical height of the first feature is lower than the vertical height of the second feature.

[0058] The present disclosure provides various embodiments and examples for implementing different structures of the present disclosure. To simplify the specification of the present disclosure, the following context just illustrates some parts and arrangements of specification embodiments.

Obviously, the described embodiments are only a part but not all of the embodiments for exemplifying the present invention instead of limiting the present invention. In addition, repeated reference numbers or letters in different embodiments are in the purpose of simplifying and clarifying, there repeated reference number or letters do not provide the suggestion of the relationship between embodiments and arrangements. All other embodiments obtained by persons of ordinary skill in the art based on the embodiments of the present invention without creative efforts shall fall within the protection scope of the present invention.

[0059] Please refer to FIG. **1**. FIG. **1** illustrates an embodiment of demultiplexer (DEMUX) display panel. The DEMUX display panel includes an array substrate **10**, a DEMUX switch **20**, a first control signal generating circuit **30**, and a second control signal generating circuit **40**.

[0060] The array substrate **10** includes a plurality of first data lines **11** intersecting a plurality of scan lines **12**. Pixel areas are defined by of a plurality of first data lines **11** intersecting a plurality scan lines **12**. Each of the pixel areas includes sub-pixels, such as red sub-pixels, blue sub-pixels, and green sub-pixels.

[0061] Each of the DEMUX switches **20** includes at least one data signal input terminal, at least two data signal output terminals, at least two first control signal input terminal and a second control signal input terminal. The data single input terminal couples to a corresponding second data line **13** to receive a data signal. Each of the at least two data signal output terminals couples to at least two sub-pixels via first data lines **11**.

[0062] The first control signal generating circuit **30** is configured to generate first control signals, and is connected to the at least two first control signal input terminal. The first control signal generating circuit **30** generates first control signals and transmit the first control signals to the corresponding first control signal input terminals so that the DEMUX switch can transmit data signals to corresponding sub-pixels via corresponding data signal output terminals.

[0063] The second control signal generating circuit **40** is configured to generate a second control signal, and is connected to the second control signal input terminal. The second control signal generating circuit **40** is configured to generate and transmit the second control signal to the DEMUX switch **20** before scanning a plurality rows of the sub-pixels, so that each of the data signal output terminals of the DEMUS switch **20** can output a reset signal to the corresponding first data line in order to reset the first data line. The reset signal is at low voltage potential.

[0064] More particularly, the DEMUX switch **20** includes at least two first transistors T**1** and at least two transistors T**2**. The number of the first transistors T**1** equals to the number of the second transistor T**2**. Both of the first transistors T**1** and second transistors T**2** are N-type field-effect transistors

[0065] An input terminal of the first transistor T**1** is coupled to a corresponding second data line **13**. An output terminal of the first transistor T**1** is coupled to the corresponding data. Each of gates of the first transistor T**1** is coupled to the first control signal generating circuit. Each of the input terminals of first transistors T**1** is coupled to an input terminal of one of the second transistor T**2**. Each of the output terminals of first transistors T**1** is coupled to an output terminal of one of the corresponding second transistor T**2**. Gates of the at least two transistors receive the second control signals.

[0066] In a first embodiment, the DEMUX switch **20** includes two first transistors T**1** and two second transistors T**2**. Correspondingly, each DEMUX switch **20** has two data signal output terminals which are coupled to two different colored sub-pixels. The two different colored sub-pixels are a red sub-pixel and a green sub-pixel, or a blue sub-pixel and a green sub-pixel.

[0067] Please refer to FIG. **2**. In a second embodiment, each DEMUX switch **20** has four data signal output terminals. The DEMUX switch has four first transistors T**1** and four second transistors T**2**. Correspondingly, the DEMUX display panel is RGBG display panel that four data signal output terminals are coupled to a red sub-pixel, a blue sub-pixel and two green sub-pixels.

[0068] In some embodiments, each DEMUX switch has three data signal output terminals which are coupled to three sub-pixels in three kinds of different colors.

[0069] Please refer to FIG. **3**, in the first and second embodiments, each sub-pixel include a first thin film transistor Q**1**, a second thin film transistor Q**2**, a third thin film transistor Q**3**, a fourth thin film transistor Q**4**, a fifth thin film transistor Q**5**, a sixth thin film transistor Q**6**, a seventh thin film transistor Q**7**, an organic light-emitting diode (OLED) D and a storage capacitor Cst. The first thin film transistor Q**1**, the second thin film transistor Q**2**, the third thin film transistor Q**3**, the fourth thin film transistor Q**4**, the fifth thin film transistor Q**5**, the sixth thin film transistor Q**6** and the seventh thin film transistor Q**7** are, but not limited, N-type field-effect transistor.

[0070] Input terminals of both of the fourth thin film transistor Q**4** and the seventh thin film transistor Q**7** receive voltage Vi. An output terminal of the fourth thin film transistor Q**4** is coupled to one end of the storage capacitor, a gate of the first thin film transistor Q**1** and an input terminal of the third thin film transistor Q**3**. Gates of both of the fourth thin film transistor Q**4** and the seventh thin film transistor Q**7** are coupled to the (n−1)th scan line. The output terminal of the fourth thin film transistor Q**4** and an output terminal of the seventh thin film transistor Q**7** are coupled to one end of the OLED D and an output terminal of the sixth thin film transistor Q**6**. Another end of the storage capacitor Cst is couple to an input terminal of the fifth thin film transistor Q**5** and receives voltage VDD. An output terminal of the fifth thin film transistor Q**5**, an output terminal of the second thin film transistor Q**2** are coupled to an input terminal of the first thin film transistor Q**1**. An output terminal of the first thin film transistor Q**1** is coupled to an output terminal Q**3** and an input terminal of the sixth thin film transistor Q**6**. A gate of the fifth thin film transistor Q**5** is coupled to a gate of the sixth thin film transistor Q**6**. A gate of the second thin film transistor Q**2** and a gate of the third thin film transistor Q**3** are coupled to the Nth scan line. An input terminal is coupled to the data line.

[0071] Please refer to FIG. **4** which illustrates the time sequence of the voltages according to the first embodiment. A reset signal Mux-reset is sent, at low voltage potential, before the scan lines start working. In the meanwhile, the second data line will receive a low voltage potential signal. Therefore the voltage potential of a corresponding first data line will be reset before charging to a corresponding row of sub-pixels. Then, first control signals Mux_EN**1** and Mux_EN**2** will be on, i.e. at high voltage potential, and will be written into practical voltage potentials of the corresponding row of sub-pixels. At the same time, the scan lines receive

corresponding scan signals Scan(n) and charge to two corresponding sub-pixels according to a data signal Data.

[0072] Please refer to FIG. **5** which illustrates the time sequence of the voltages according to the second embodiment shown in FIG. **2**. A reset signal Mux-reset is sent, at low voltage potential, before the scan lines start working. In the meanwhile, the second data line will receive a low voltage potential signal. Therefore the voltage potential of a corresponding first data line will be reset before charging to a corresponding row of sub-pixels. Then, the first control signals Mux-EN**1**, Mux-EN**2**, Mux-EN**3**, and Mxu-EN**4** will be written into practical voltage potentials of the corresponding row of sub-pixels. At the same time, the scan lines receive corresponding scan signals Scan(n) and charge to four sub-pixels corresponding to the first data lines.

[0073] The present disclosure further provides a OLED display which comprises any one of the DEMUX display panel of above-mentioned embodiments.

[0074] By utilizing the second control signal generating circuit, which is connected to the second control signal input terminals, the second control signal will be generated and transmitted to the DEMUX switches so that the DEMUX switches will send reset signals to the corresponding first data line in order to reset the first data lines before charging the sub-pixels. Therefore, problems of written error resulted from the influence caused from the (n−1)th data line because the voltage potential of the (n−1)th first data line is higher than the voltage potential of the nth first data line. As a result, beneficial effect is created because the display error is avoided.

[0075] The detailed introduction of the embodiments of the DEMUX display panel and OLED display of present disclosure are illustrated as above-mention context. The specification illustrates the technologies and implementing methods of the present disclosure. Although this disclosure has been disclosed through the preferable embodiments above, the preferable embodiments above are not utilized to limit this disclosure. One having ordinary skills can change and modify without violating the concepts and scope of this disclosure. Therefore, the scope that this disclosure protects should not be limited by the embodiments in specification and should base on the scope defined by the claims.

1. A demultiplexer (DEMUX) display panel, comprising:

an array substrate comprising a pixel area defined by a plurality of first data lines intersecting a plurality of scan lines, wherein the pixel area comprises sub-pixels;

a plurality of DEMUX switches, each of the DEMUX switches comprising at least one data signal input terminal, at least two data signal output terminals, at least two first control signal input terminals, and a second control signal input terminal, wherein a corresponding second data line connects to the data signal input terminal, the corresponding first data lines connects between the at least two data signal output terminals and at least two of the sub-pixels;

a first control signal generating circuit connected to the at least two first control signal input terminals, and configured to generate a first control signal, wherein the first control signal is sent to one of the corresponding first control signal input terminals to make the DEMUX switch transmit a data signal to the corresponding sub-pixels through a corresponding data signal output terminal;

a second control signal generating circuit connected to the second control signal input terminal, and configured to generate a second control signal, wherein the second control signal is sent to the DEMUX switch before scanning the sub-pixels to make the DEMUX switch transmit a reset signal to the corresponding first data lines through both of the data signal output terminals;

wherein the DEMUX switch comprises at least two first transistors and at least two second transistors;

wherein an input terminal of the first transistor connects to the corresponding second data line, an output terminal of the first transistor connects to one of the corresponding data line and the corresponding sub-pixels, a gate of the first transistor connects to the first control signal generating circuit;

wherein the input terminals of both of the first transistors connect to input terminal of the second transistors, the output terminals of both of the first transistors connect to output terminals of the corresponding second transistors, gates of the at least two second transistors connect to each other to receive the second control signal;

each of the DEMUX switches comprises two data signal output terminals connected to two different colored sub-pixels.

2. The DEMUX display panel according to claim **1**, wherein the first transistors and the second transistors are N-type thin film transistors.

3. The DEMUX display panel according to claim **1**, wherein the two different colored sub-pixels are a red sub-pixel and a green sub-pixel, or the two different colored sub-pixels are a blue sub-pixel and a green sub-pixel.

4. The DEMUX display panel according to claim **3**, wherein the data signal output terminals of the DEMUX switches transmit low potential voltages as the reset signal to the corresponding second data line before scan lines receive scan signals.

5. The DEMUX display panel according to claim **1**, wherein each of the DEMUX switches comprises four data signal output terminals connected to a red sub-pixel, a blue sub-pixel and two green sub-pixels.

6. The DEMUX display panel according to claim **1**, wherein each of the DEMUX switches comprises three data signal output terminals connected to a red sub-pixel, a blue sub-pixel and a green sub-pixel.

7. The DEMUX display panel according to claim **1**, wherein each of the sub-pixels comprises a first thin film transistor, a second thin film transistor, a third thin film transistor, a fourth thin film transistor, a fifth thin film transistor, a sixth thin film transistor, a seventh thin film transistor, an organic light-emitting diode, and a storage capacitor;

wherein an input terminal of the fourth thin film transistor and an input terminal of the seventh thin film transistor receive a Vi voltage, an output terminal of the fourth thin film transistor connects to a first terminal of the storage capacitor, a gate of the first thin film transistor and an input terminal of the third thin film transistor, a gate of the fourth thin film transistor and a gate of the seventh thin film transistor connect to an (n−1)th scan line, the output terminal of the fourth thin film transistor and an output terminal of the seventh thin film transistor connect to the organic light-emitting diode and an output terminal of the sixth thin film transistor,

a second terminal of the storage capacitor connects to an input terminal of the fifth thin film transistor and receives a VDD voltage, an output terminal of the fifth thin film transistor and an output terminal of the second thin film transistor connect to an input terminal of the first thin film transistor, in output terminal of the first thin film transistor connects to an output terminal of the third thin film transistor and an input terminal of the sixth thin film transistor, a gate of the fifth thin film transistor connects to a gate of the sixth thin film transistor, a gate terminal of the second thin film transistor connects to a gate of the third thin film transistor and the (n)th scan line, an input terminal of the second thin film transistor connects to one of the corresponding first data lines.

8. A demultiplexer (DEMUX) display panel, comprising:

an array substrate comprising a pixel area defined by a plurality of first data lines intersecting a plurality of scan lines, wherein the pixel area comprises sub-pixels;

a plurality of DEMUX switches, each of the DEMUX switches comprising at least one data signal input terminal, at least two data signal output terminals, at least two first control signal input terminals, and a second control signal input terminal, wherein a corresponding second data line connects to the data signal input terminal, the corresponding first data line connects between the at least two data signal output terminals and at least two of the sub-pixels;

a first control signal generating circuit connected to the at least two first control signal input terminals, and con figured to generate a first control signal, wherein the first control signal is sent to one of the corresponding first control signal input terminals to make the DEMUX switch transmit a data signal to the corresponding sub-pixels through a corresponding data signal output terminal;

a second control signal generating circuit connected to the second control signal input terminal, and con figured to generate a second control signal, wherein the second control signal is sent to the DEMUX switch before scanning the sub-pixels to make the DEMUX switch transmit a reset signal to the corresponding first data lines through both of the data signal output terminal.

9. The DEMUX display panel according to claim **8**, wherein the DEMUX switch comprises at least two first transistors and at least two second transistors;

wherein an input terminal of the first transistor connects to the corresponding second data line, an output terminal of the first transistor connects to one of the corresponding first data line and the corresponding sub-pixels, a gate of the first transistor connects to the first control signal generating circuit;

wherein the input terminals of both of the first transistor connects to input terminals of the second transistors, the output terminals of both of the first transistor connect to output terminals of the corresponding second transistors, gates of the at least two second transistors connect to each other to receive the second control signal.

10. The DEMUX display panel according to claim **9**, wherein the first transistors and the second transistors are N-type thin film transistor.

11. The DEMUX display panel according to claim **8**, wherein each of the DEMUX switches comprises two data signal output terminals connected to two different colored sub-pixels.

12. The DEMUX display panel according to claim **11**, wherein the two different colored sub-pixels are a red sub-pixel and a green sub-pixel, or the two different colored sub-pixels are a blue sub-pixel and a green sub-pixel.

13. The DEMUX display panel according to claim **12**, wherein the data signal output terminals of the DEMUX switches transmit low potential voltages as the reset signal to the corresponding second data line before scan lines receive scan signals.

14. The DEMUX display panel according to claim **8**, wherein each of the DEMUX switches comprises four data signal output terminals connected to a red sub-pixel, a blue sub-pixel and two green sub-pixels.

15. The DEMUX display panel according to claim **8**, wherein each of the DEMUX switches comprises three data signal output terminals connected to a red sub-pixel, a blue sub-pixel and a green sub-pixel.

16. The DEMUX display panel according to claim **8**, wherein each of the sub-pixels comprises a first thin film transistor, a second thin film transistor, a third thin film transistor, a fourth thin film transistor, a fifth thin film transistor, a sixth thin film transistor, a seventh thin film transistor, an organic light-emitting diode, and a storage capacitor;

wherein an input terminal of the fourth thin film transistor and an input terminal of the seventh thin film transistor receive a Vi voltage, an output terminal of the fourth thin film transistor connects to a first terminal of the storage capacitor, a gate of the first thin film transistor and an input terminal of the third thin film transistor, a gate of the fourth thin film transistor and a gate of the seventh thin film transistor connect to an (n−1)th scan line, the output terminal of the fourth thin film transistor and an output terminal of the seventh thin film transistor connect to the organic light-emitting diode and an output terminal of the sixth thin film transistor, a second terminal of the storage capacitor connects to an input terminal of the fifth thin film transistor and receives a VDD voltage, an output terminal of the fifth thin film transistor and an output terminal of the second thin film transistor connect to an input terminal of the first thin film transistor, in output terminal of the first thin film transistor connects to an output terminal of the third thin film transistor and an input terminal of the sixth thin film transistor, a gate of the fifth thin film transistor connects to a gate of the sixth thin film transistor, a gate of the second thin film transistor connects to a gate of the third thin film transistor and the (n)th scan line, an input terminal of the second thin film transistor connects to one of the corresponding first data lines.

17. A organic light-emitting diode (OLED) display comprising a demultiplexer (DEMUX) display panel,

the DEMUX display panel comprises:

an array substrate comprising a pixel area defined by a plurality of first data lines intersecting a plurality of scan lines, wherein the pixel area comprises sub-pixels;

a plurality of DEMUX switches, each of the DEMUX switches comprising at least one data signal input terminal, at least two data signal output terminals, at

least two first control signal input terminals, and a second control signal input terminal, wherein a corresponding second data line connects to the data signal input terminal, the corresponding first data lines connects between the at least two data signal output terminals and at least two of the sub-pixels;

a first control signal generating circuit connected to the at least two first control signal input terminals, and con figured to generate a first control signal, wherein the first control signal is sent to one of the corresponding first control signal input terminals to make the DEMUX switch transmit a data signal to the corresponding sub-pixels through a corresponding data signal output terminal;

a second control signal generating circuit connected to the second control signal input terminal, and con figured to generate a second control signal, wherein the second control signal is sent to the DEMUX switch before scanning the sub-pixels to make the DEMUX switch transmit a reset signal to the corresponding first data lines through both of the data signal output terminal;

18. The OLED display according to claim **17**, wherein the DEMUX switch comprises at least two first transistors and at least two second transistors;

wherein an input terminal of the first transistor connects to the corresponding second data line, an output terminal of the first transistor connects to one of the corresponding first data line and the corresponding sub-pixels, a gate of the first transistor connects to the first control signal generating circuit;

wherein the input terminals both of the first transistor connects to an input terminal of one of the second transistors, the output terminals both of the first transistor connects an output terminal of the corresponding second transistor, gates of the at least two second transistors connect to each other to receive the second control signal.

19. The OLED display according to claim **18**, wherein the first transistors and the second transistors are N-type thin film transistor.

20. The OLED display according to claim **17**, wherein each of the DEMUX switches comprises two data signal output terminals connected to two different colored sub-pixels.

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专利名称(译)	多路分解显示面板和OLED显示器		
公开(公告)号	US20200126489A1	公开(公告)日	2020-04-23
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[标]发明人	ZENG MIAN		
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摘要(译)

一种解复用器（DEMUX）显示面板，包括阵列基板，多个DEMUX开关和第二控制信号生成电路，该第二控制信号生成电路连接至第二控制信号输入端子并被配置为生成第二控制信号。 在扫描子像素的每一行之前，将第二控制信号发送到DEMUX开关，以使DEMUX开关通过两个数据信号输出端子将复位信号发送到相应的第一数据线。